REMARKS

Through this Reply, Applicants have amended Claims 25 and 31. Accordingly, Claims 25-33 are active in the present application. The Amendments to Claims 25 and 31 are supported in the specification on at least page 8, line26 through page 9, line 1, page 11, lines 7-9, and page 11, lines 25-29 of the present specification. In the specification, the layer insulating film 11 has been amended to the interlayer insulating film 11 based on the description on page 11, lines 25-29. Accordingly, no new matter has been added by this amendment.

The Examiner has rejected Claims 31-33 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time of the invention, had possession of the claimed invention. Specifically, the Examiner asserts that there is no support for a modified SOG film formed by implanting boron impurity into an inorganic SOG film. Applicants respectfully traverse the rejection. Specifically, Applicants note that support for the claim limitation "including a first insulating film that is a modified spin-on-glass (SOG) film formed by implanting boron impurity into an inorganic SOG film" is supported in the specification on at least page 17, lines 17-19. Accordingly, Applicants submit that Claims 31-33 are allowable.

The Examiner has rejected Claims 25-33 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,984,055 to Okumura et al. (hereinafter "Okumura"), or Japanese Patent No. 6-291202 (herinafter "the '202 reference"). Applicants have amended claims 25 and 31 to more particularly point out the claimed invention. The present invention, as claimed by independent claims 25 and 31, is directed to a semiconductor device that includes a passivation

film located to cover the surface of an interlayer insulating film and wirings. The passivation film includes a first insulating film that is a modified spin-on-glass (SOG) film formed by inplanting boron impurity into in organic SOG film (claim 25) of an inorganic SOG film (claim 31).

Okumura discloses a semiconductor device having an SOG layer (13) as in interlayer insulation film. A boron impurity is ion-implanted into the SOG layer (13) in order to increase its etching resistivity. However, Okumura does not teach or suggest a passivation film that covers the surface of an interlayer insulating layer and wirings in order to have improved moisture resistance. Okumura discloses a polysilicon layer (16) as a wiring layer located on the SOG layer (13), and do not disclose a passivation film located on the polysilicon layer (16). Accordingly, for at least this reason, Applicants submit that Claims 25 and 31are patentably distinguishable from Okumura. Furthermore, Applicants submit that claims 26-30, and claims 32-33, which depend (directly or indirectly) from claim 25 or 31, are likewise patentably distinguishable for at least the same reason.

The '202 reference is directed to a semiconductor device that includes a lower boron and phosphorous doped SOG layer (15) and an upper non-doped SOG layer (16) located on an interlayer insulation film (14). The upper non-doped SOG layer (16) prevents phosphorous in the SOG layer (15) from reacting with moisture in the atmosphere. However, the '202 reference does not teach or suggest a passivation film that covers the surface of an interlayer insulating layer and wirings to protect the wirings from moisture. The wirings (13) in the '202 reference are covered by the interlayer insulating file (14), but not the lower boron and phosphorous doped SOG layer (15). Since, as claimed in claims 25 and 31, the wirings of the present invention are

located on the interlayer insulating film, the passivation film is provided to cover the wirings and the interlayer insulating film. Accordingly, Applicants submit that independent claims 25 and 31 are patentably distinguishable from the '202 reference. Furthermore, Applicants submit that Claims 26-30 and 32-33, which depend (directly or indirectly) from claims 25 or 31, are likewise in condition for allowance for at least the same reasons.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

The paragraph starting at page 8, line 26 has been replaced with the following replacement paragraph:

The first embodiment employs the sandwich structure in which the modified SOG film 7 is sandwiched between the silicon oxide films 5 and 8, which enhances the insulating properties and mechanical strength of the [layer] interlayer insulating film 11 as a whole. Further, since the modified SOG film 7 contains no organic component, the etching treatment for forming the via holes 9 is carried out in a mixed gas atmosphere of carbon tetraflouride and hydrogen. Accordingly, even if a photoresist is employed as an etching mask, the photoresist is not attacked, nor is the modified SOG film 7 masked with the photoresist etched. Thus, fine via holes 9 are formed accurately.

The paragraph starting at page 11, line 7 has been replaced with the following replacement paragraph:

As described above, according to the second embodiment, the wirings 23 are formed on the source and drain wirings 10 via the [layer] interlayer insulating film 11. In this case again, the same actions and effects as in the first embodiment can be exhibited without effecting the MOS transister and source and drain wirings 10.

In The Claims:

Claims 25 and 31 have been amended as follows:

25. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an interlayer insulating film located on the semiconductor substrate;

wirings located on the [semiconductor substrate] interlayer insulating film; and

a passivation film covering the surface of the [semiconductor substrate] interlayer insulating film and the wirings, including a first insulating film that is a modified spin-on-glass (SOG) film formed by implanting boron impurity into an organic SOG film.

31. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an interlayer insulating film located on the semiconductor substrate;

wirings located on the [semiconductor substrate] interlayer insulating film; and

a passivation film covering the surface of the [semiconductor substrate] interlayer insulating film and the wirings, including a first insulating film that is a modified spin-on-glass (SOG) film formed by implanting boron impurity into an inorganic SOG film.